Supplementary Data Description

Overview

This document aims to providing some additional data regarding all the research about our proposed inverter-based OTA. The readers will find out useful information about the I.C. implementation, in Section 1, measurement setups in Section 2, and experimental raw data in Section 3. In addition, we have produced a video documentary showing the Laboratory of Tests and Characterization on Microelectronics (LTCaM) where all the measurements took place. Section 4 provides additional information about the video production.

1. Integrated Circuit implementation

The inverter-based OTA integrated circuit, illustrated in Fig. A, was fabricated trough the MOSIS consortium using the GF_8RF wafer technology. The fabrication run occurred on 16-MAY-2016, under the Fab ID V65K-AL, of which, our design was identified by the Design No. 93886. In addition, the Appendix A provides all the foundry documentation that attest the fabrication of the project as follows: (*i*) final bounding diagram, (*ii*) MOSIS Project Management page related to the project, and (*iii*) report of our orders including the conclusion of the process.

2. Measurement setup

This section details the measurement setups we have used to characterize the inverter-based OTA integrated circuit in the manuscript: additional schematics of external circuits and additional information about the measurement equipment. Each test has its on subsection that follows the same order we presented in the paper to make the evaluation easier.

2.1. Frequency response

Figure B shows the frequency response measurement setup. The Keysight 35670A Dynamic Signal Analyzer (DSA) has been configured to perform a **Sweep Sine** test. Since the DSA provides only one low-distortion signal source we have applied it to the INA129(1) in the gain configuration, set up with a gain of – 1 [V/V], hence, providing a secondary source with inverted output, which is necessary to perform a full differential measurement. According to the DSA user guide, regarding the frequency response measurement, we must apply the input voltage to CH1 channel and the output voltage (measurement target) to the CH2 channel, therefore, we have used both INA129(2) and INA129(3) to convert the differential voltages to single-ended ones before applying them to the DSA respective channels.

Furthermore, DSA the signal source have been configured for an output voltage of $V_o = 125.0 + 1.0\sin(2\pi 10t)$ [mV] giving $2.0\sin(2\pi 10t)$ [mV] fully differential voltage applied to the OTA inputs.

In addition, either the INA129 parts or the OTA integrated circuit are supplied by a Hewlett Packard E3631A power source that provides ± 15 [V] lines for the INA129 and a 250 [mV] line for the OTA.

2.2. Differential current

Figure C illustrates the measurement setup for the output differential current. This setup uses a Keysight B1500A semiconductor analyzer which provides four source meter units (SMU), where the SMU1 - SMU2 are connected to the non-inverter and inverter OTA inputs, respectively, and the SMU3 - SMU4 are connected to the OTA outputs. While the SMU1 sweeps the non-inverting input from – 125 [mV] to 125 [mV] with steps of 500 [μV], the SMU2 performs the opposite, sweeping the inverting input from 125 [mV] to – 125 [mV] with steps of – 500 [μV]. Furthermore, the SMU3 and SMU4 are configured as constant voltage sources of 125 [mV] to keep the appropriate common mode voltage while they measure the current of each output node. Therefore, the measured output differential current is $I_{od} = I_{SMU4} - I_{SMU3}$. In addition, we used a Hewlett Packard E3631A power source to supply the inveter-based OTA with 250 [mV].

2.3. Input-referred noise density

Figure D depicts the measurement setup for the input-referred noise density measurement which uses two SMUs from the B1500A configured as constant voltage sources with 125 [mV] at both the OTA inputs. We have used the INA129(1), configured with an unitary gain, at the OTA outputs in order to convert it to a single-ended signal, which we connected to CH1 channel of the DSA Furthermore, the DSA has been configured to measure the power spectral density according to the user guide. We wolud like to highlight that both INA129(1) and 35670A present a noise floor, at least, 1000 times smaller than our inverter-based OTA, hence, they do not affect the measurement results. In addition, either the INA129 or the OTA integrated circuit are supplied by a Hewlett Packard E3631A power source that provides ± 15 [V] lines for the INA129 and a 250 [mV] line for the OTA.

2.4. Lossy G_m-C Integrator

Figure E presents the measurement setup for transient response of the lossy G_m-C integrator configuration. The INA129 parts are configured in the same way of subsection 2.1. However, in this setup we have an Agilent 33210A signal generator, a Keysight DSOS04A infiniium S-sereis oscilloscope, and load capacitances of 22 [nF]. In addition, either the INA129 or the OTA integrated circuit are supplied by a Hewlett Packard E3631A power source that provides ± 15 [V] lines for the INA129 and a 250 [mV] line for the OTA.

Figure F shows the measurement setup for harmonic distortion where The 35670A DSA was configured to perform a *power spectrum measurement*. The signal source have been configured for an output voltage of $V_o = 125.0 + 9.4\sin(2\pi 10t)$ [mV], which leading to $18.8\sin(2\pi 10t)$ [mV] at the OTA inputs after using the INA129(1) to obtain a secondary signal source with inverted outputs. The INA129(2), placed at the OTA outputs, converts the OTA differential output signal to a single-ended signal which is applied to the CH1 channel of the DSA. In addition, either the INA129 or the OTA integrated circuit are supplied by a Hewlett Packard E3631A power source that provides ± 15 [V] lines for the INA129 and a 250 [mV] line for the OTA.

3. Experimental raw data

This section lists all the raw data we have collected along the characterization procedure. They are placed inside the "*supplementary_data.zip*" file. Since the raw data comprehends a plethora of .csv files, we provided a simple description for each one, as follows:

- The "*figure_3*" folder contains the voltage transfer characteristics simulation ("*figure_3a*") and its derivative ("*figure_3b*") for the CMOS inverters. Each .csv file holds x-axis and y-axis data for the intrinsically matched CMOS inverters 1x1, 2x2, 4x4 and 8x8 and theirs joint equivalent.

- The "*figure_4*" folder contains voltage switching point V_{SP} Monte Carlo results for the self-connected intrinsically matched CMOS inverters 1x1, 2x2, 4x4 and 8x8 and theirs joint equivalent. Each .csv file holds the run number and the V_{SP} value.

- The "*figure_7*" folder contains the inverter-based OTA measured frequency response results. The sub-folders "*figure_7a*", "*figure_7b*" and "*figure_7c*" hold the frequency response results for the inverter-based OTA 2x2, 4x4 and 8x8, respectively. Inside these sub-folders there are (*i*) a single x-axis frequency file, (*ii*) a gain and phase file for each sample and (*iii*) the typical frequency response files.

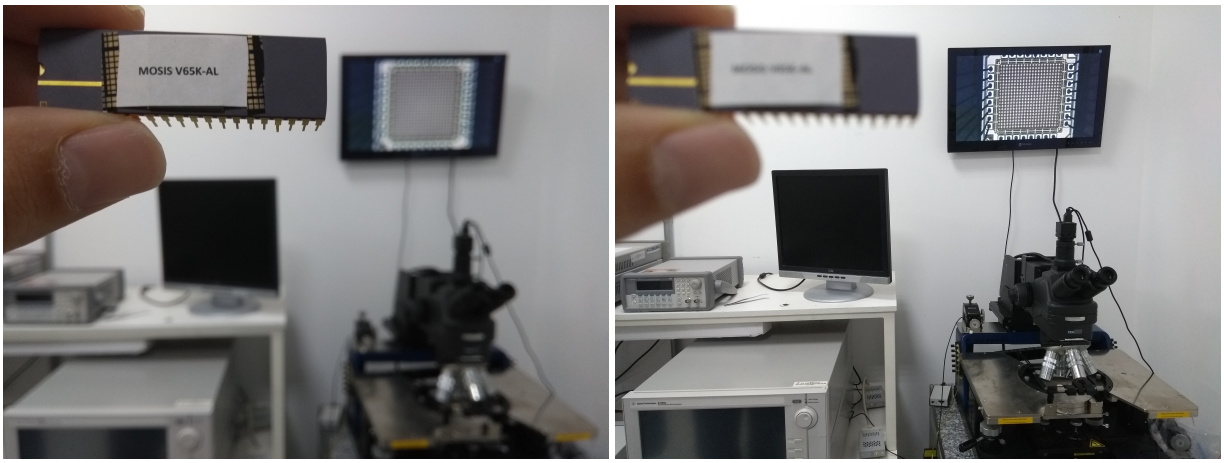
- The "*figure_8*" folder contains the inverter-based OTA measured results for the differential current. Inside this folder are placed (*i*) a single x-axis file ("*vin.csv*") and (*ii*) the y-axis differential current files for the highest and lowest transconductance values.

- The "*figure_9*" folder contains the inverter-based OTA measured results for the input-referred noise density. Inside this folder are placed (*i*) a single x-axis frequency file and (*ii*) the y-axis files for the highest and lowest noise floor thermal densities.

- The "*figure_10*" folder contains the lossy G_m-C filter transient response excited by a square wave input signal. Inside this folder are placed (*i*) a single x-axis file for time and (*ii*) the y-axis files for the input square wave and output from lossy G_m-C filter.
- The "*figure_11*" folder contains the lossy G_m-C filter measured frequency response results. Inside this folder there are (*i*) a single x-axis frequency file and (*ii*) the gain and phase files for lossy G_m-C frequency response.
- The "*figure_12*" folder contains the lossy G_m-C filter measured harmonic distortion results. Inside this folder there are (*i*) a single x-axis frequency file and (*ii*) the y-axis spectrum file for lossy G_m-C harmonic distortion response.

4. Video documentary

The video documentary was recorded on 26th September, 2018 in the Laboratory of Tests and Characterization on Microelectronics (LTCaM), part of the Microelectronics Group of the Federal University of Itajubá, where the research has been conducted. In this video we show all the equipment and devices used in our test bench and perform the measurement of the lossy G_m-C integrator. We hope you enjoy the video.



(a) Focusing the integrated circuit, highlighting the fabrication ID from MOSIS, V65K-AL.

(b) Focusing the measurement equipment showing the die in the display. Since the Integrated circuit has an opaque top layer, we are showing the complete pad frame.

Figure A: Integrated circuit implementation view using a Cascade Microtech MPS 150.

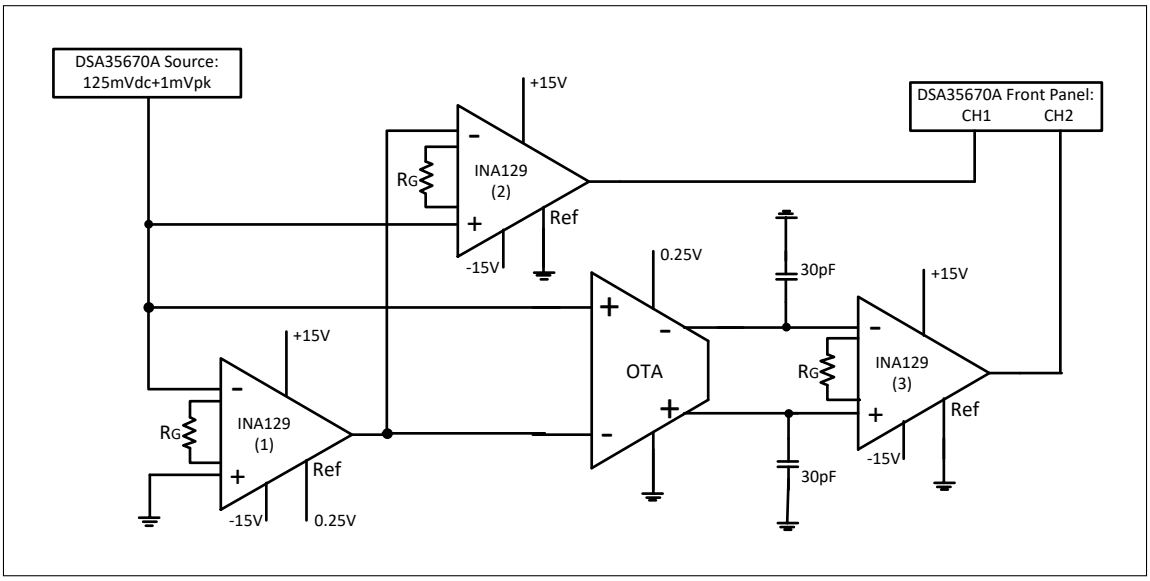


Figure B: Test bench for frequency response.

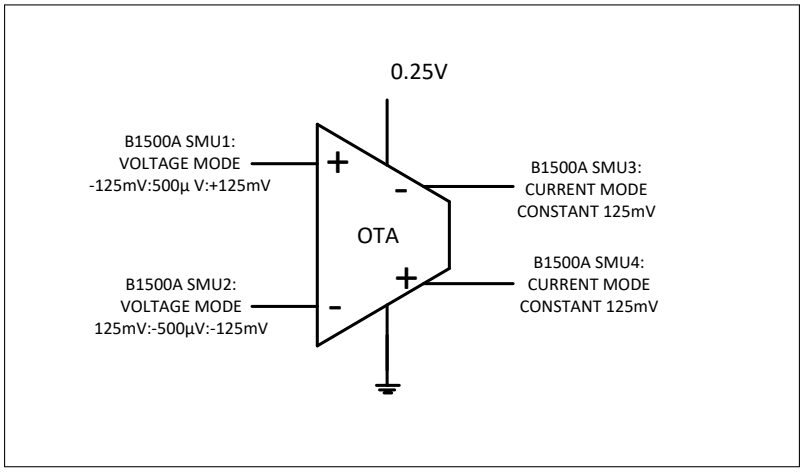


Figure C: Test bench for the output differential current.

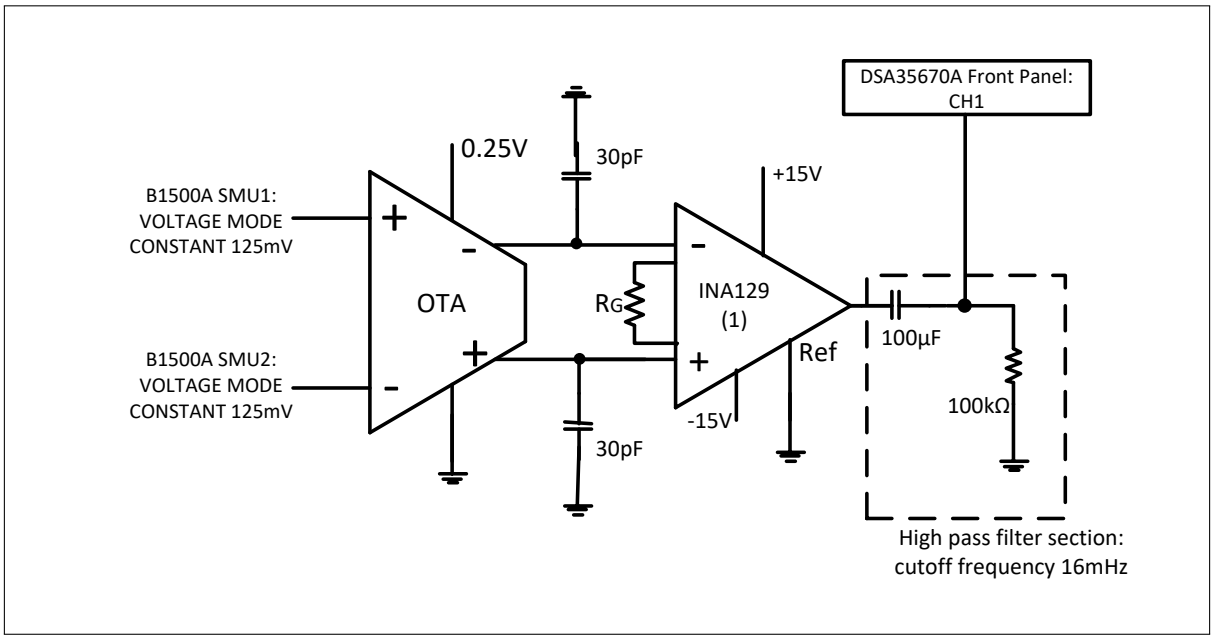


Figure D: Test bench for input-referred noise density.

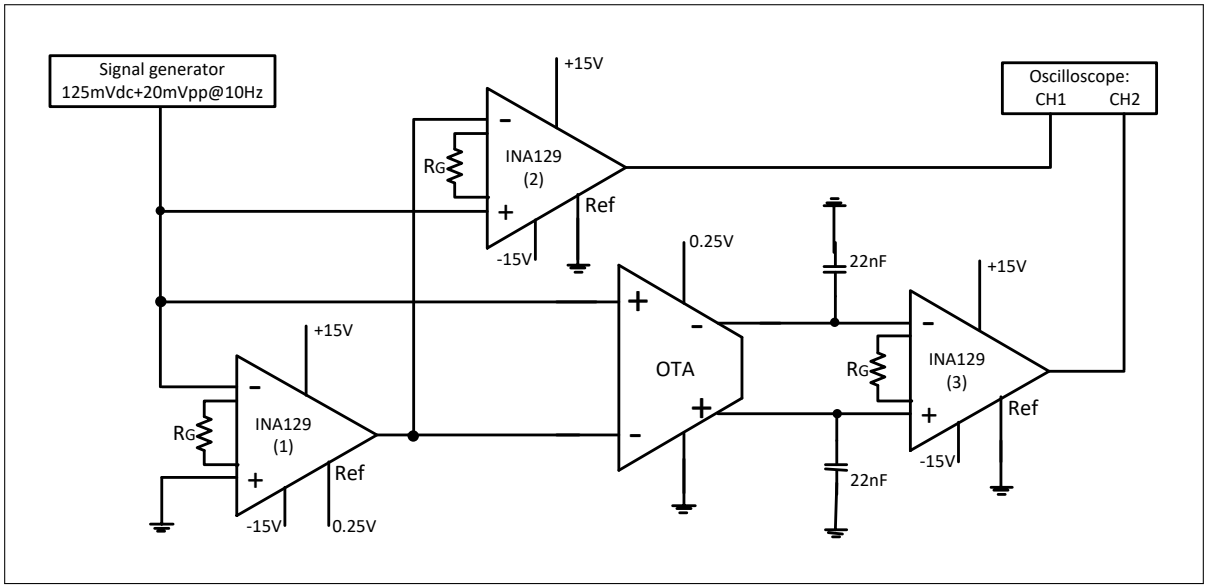


Figure E: Transient test bench for lossy G_m-C integrator.

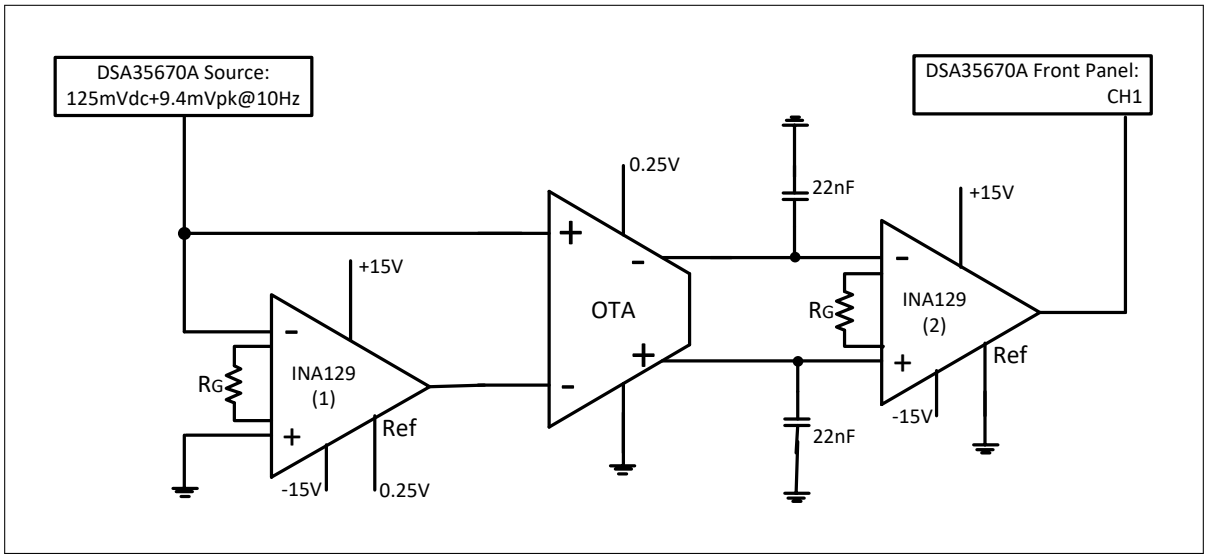
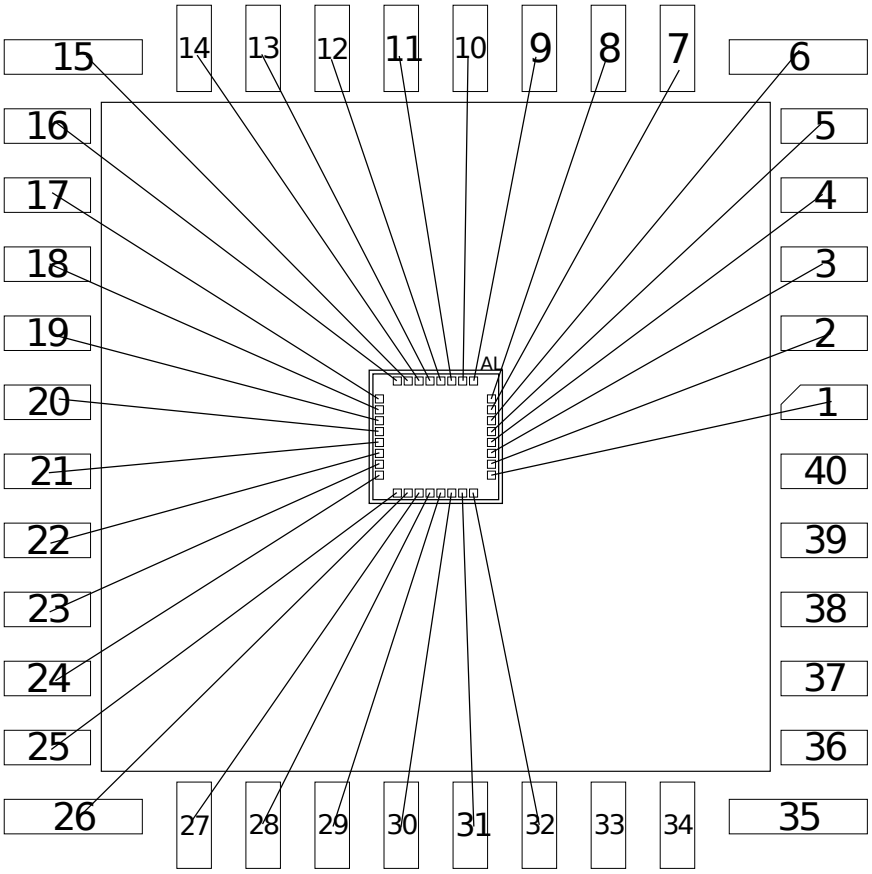


Figure F: Harmonic distortion test bench for lossy G_m-C integrator.

Appendix A

A.1 - Bounding diagram



Qty: 40	V65K-AL (93886)	DIP40
Customer Providing Diagram Minimum pad size: 95 x 95; minimum pad pitch: 128 um		20 — 1 TOP VIEW 21 — 40
MOSIS	Design_name: inversor_block Customer Account: 5817 Die Size: 1568 x 1568 um Die Rotation in Cavity: None Cavity Size: 7874 um x 7874 um	27-J UN-2016 16:11:42

A.2 - Project management page

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Project Information

Design Number	***93886***
Date Created	07-MAR-16 11:39:43 am
Project Status	***Shipped***
Design Layout	Final layout
Fab ID	V65KAL
Project Document(s)	***Download***
Fabrication Options	***8LM, MG/LY/E1/MA, WIREBOND***
Run Date Requested	16-MAY-2016
Area	2.19 sq millimeters
Checksum	Binary CRC checksum: 975183728, Binary CRC byte count: 3239936

Administrative Information

Account Name	5817-MEP-INS/UFDI-ITABIRA
Account Contact Name	Rodrigo Braga
Account Contact E-mail	rodrigobraga@unifei.edu.br
Technical Point Contact Name	Rodrigo Braga
Technical Point Contact E-mail	rodrigobraga@unifei.edu.br
Design Contact E-mail	rodrigobraga@unifei.edu.br
Design Contact Phone	
Cost	V65K: 1 MEP unit(s) is used.
Quantity Ordered	40
ECCN	EAR99 -- This design implementation provides inversors circuits builded as an array of CMOS transistors. The intended application of this design is study the behavior of this inversors array as analog amplifiers operating in subthreshold region. Technology ECCN: EAR99
USECQ received	Yes
Approved for export	Yes

Design Details

Size in X	1480
Size in Y	1480
Wafer Technology	GF_8RF
Layout Format	GDS
Top Cell Name	frame_8x8_final_rotacionado
Fill	Foundry
Bonding Pad Count (Customer)	32
Bonding Pad Count (MOSIS)	32
Maximum Die Size	7620.0 X 7620.0
Layers (Density)	ALPHAPAD, BFMOAT, BFMOATIND, BONDPAD, BP, CA, CABAR, CHIPEDGE, DV, E1, ESDCDM, ESDIODE, ESDUMMY, F1, F1BAR, FT, FTBAR, FY, FYBAR, GUARDRNG, LOGOBND, LY, M1, M2, M2_ESDF, M3, MA, MG, MQ, MULTIDEV, NW, OP, PADPAD, PC, PROTECT, RP, RX, V1, V1BAR, V1_ESDF, V2, V2BAR, VL, VLBAR, VQ, VQBAR

Packaging Information

Quantity	Packaged	Package Id	Bonding Diagram Received	Bonding Diagram From	Die Thickness (mils)	Production ID Date Shipped
40	Y	DIP40	28-JUN-16	Customer	10	V65K 12-SEP-16

Project Warnings

Warning	189 text nodes ignored on layers: 15,63,81,200 (This warning indicates an anomaly in the file that does not compromise our processing of the data.)

Shipping Status

Shipping Status	Date Shipped	Production ID/PO Number	Tracking #	Shipping Address
Shipped	12-SEP-16	V65K / CA 5817 FY16	75 7111 4305	Rodrigo Aparecido Braga Univeridade Federal de Itajuba Itabira Campus

A.3 - Report of orders

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Orders In Progress

For Shared IC Fabrication Runs

Prod ID	Fab ID	Date Ordered	Design No.	Design Name	Test Report	Report Reminder Sent
V7BB	V7BB-CY	04-Oct-2017	96662	inverters_nauta	N/A	

Completed Orders

For Shared IC Fabrication Runs

Prod ID	Fab ID	Date Ordered	Design No.	Design Name	Test Report	Report Reminder Sent
V65K	V65K-AL	07-Mar-2016	93886	inversor_block	N/A	